DALLAS SEMICONDUCTOR

DS21600/2/4
Clock Rate Adapter

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FEATURES

- Direct drop-in replacement for LXP600ASE, LXP602SE, and LXP604SE
- Converts E-carrier clock rates to T-carrier clock rates
- Converts T-carrier clock rates to E-carrier clock rates
- Low jitter output
- Multiple output clocks synchronized to input clock
- 8kHz frequency-locked output for all modes of operation
- No external components required
- 16-pin SOIC and 8-pin DIP

ORDERING INFORMATION

DS21600SN	16-Pin SOIC	(-40°C to +85°C)
DS21600N	8-Pin DIP	(-40°C to +85°C)
DS21602SN	16-Pin SOIC	(-40°C to +85°C)
DS21602N	8-Pin DIP	(-40°C to +85°C)
DS21604SN	16-Pin SOIC	(-40°C to +85°C)
DS21604N	8-Pin DIP	(-40°C to +85°C)

FREQUENCY CONVERSIONS (MHz)

	CLKIN	CLKOUT1	CLKOUT2
DS21600	1.544	2.048	6.144
	2.048	1.544	6.176
DS21602	1.544	2.048	8.192
	2.048	1.544	6.176
DS21604	1.544	4.096	8.192
	4.096	1.544	6.176

DESCRIPTION

The DS21600, DS21602, and DS21604 are multi-rate clock adapters that convert between E-carrier and T-carrier clocks rates. These devices are available in 16-pin SOIC and are rated for industrial temperatures. A T1 or E1 clock output is available, CLKOUT1, along with a higher multiple rate, CLKOUT2. CLKOUT1 and CLKOUT2 are frequency-locked to the clock input, CLKIN. The clock outputs, along with frame-sync output, can be phase-aligned to a frame-sync input. The devices are fully compatible to the LXP600A, LXP602, and LXP604 and operate from a single 5V supply. All operation modes include a standard 8kHz output.

TABLE OF CONTENTS

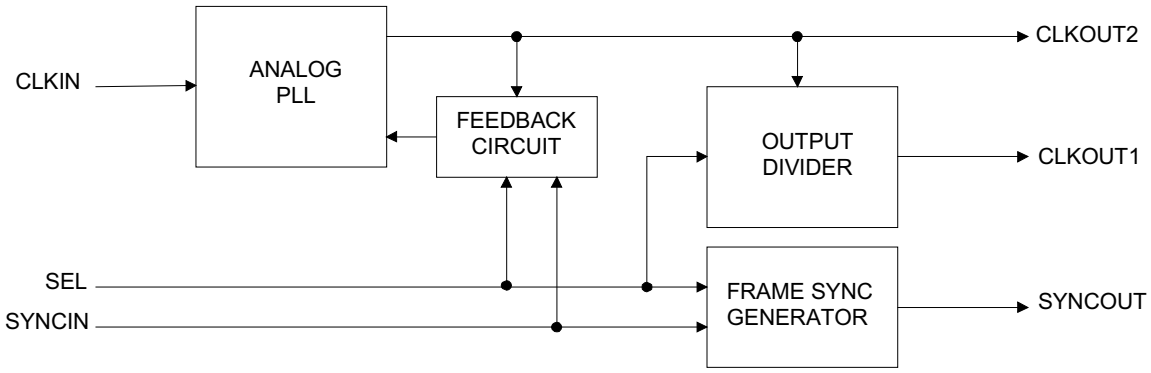
LIST OF TABLES

LIST OF FIGURES

FUNCTIONAL DESCRIPTION

A clock input at CLKIN is converted to an alternate clock rate available on CLKOUT1. A higher multiple rate clock also is available on CLKOUT2. Additionally, an 8kHz clock locked to CLKIN is always available at the SYNCOUT pin. The SEL pin controlls clock rate conversion selection.

DS2160x BLOCK DIAGRAM Figure 1



PIN FUNCTION DESCRIPTION

Signal Name: **CLKIN**
Signal Description: **Clock Input**
Signal Type: **Input**
Reference Clock Input. CLKOUT1 and CLKOUT2 will be referenced to this clock.

Signal Name: **CLKOUT1**
Signal Description: **Clock Output 1**
Signal Type: **Output**
T1 or E1 carrier clock output referenced to CLKIN.

Signal Name: **CLKOUT2**
Signal Description: **Clock Output 2**
Signal Type: **Output**
T1 or E1 carrier clock output referenced to CLKIN.

Signal Name: **SEL**
Signal Description: **Clock Mode Select**
Signal Type: **Input**
Conversion mode select

Signal Name: **SYNCIN**
Signal Description: **Synchronization Input**
Signal Type: **Input**
Used to synchronize the clock outputs and SYNCOUT to CLKIN and SYNCIN.

Signal Name: **SYNCOUT**
Signal Description: **Synchronization Output**
Signal Type: **Output**
An 8kHz output that can be synchronized to the clock outputs.

Signal Name: **V_{DD}**
Signal Description: **Positive Supply**
Signal Type: **Supply**
5.00V ±5%

Signal Name: **V_{SS}**
Signal Description: **Signal Ground**
Signal Type: **Supply**
Ground

PIN DESCRIPTION SORTED BY PIN NUMBER Table 1

PIN # 16-PIN SOIC	PIN # 8-PIN DIP	PIN NAME	TYPE	DESCRIPTION
1	-	N/C	-	NO CONNECT
2	1	SYNCOUT	O	Synchronization Pulse Output
3	-	N/C	-	NO CONNECT
4	2	CLKOUT2	O	Clock 2 Output
5	3	CLKIN	I	Clock Input
6	-	N/C	-	NO CONNECT
7	4	CLKOUT1	O	Clock 1 Output
8	-	N/C	-	NO CONNECT
9	5	V_{SS}	-	Ground
10	-	N/C	-	NO CONNECT
11	-	N/C	-	NO CONNECT
12	6	SEL	I	Clock Mode Select
13	-	N/C	-	NO CONNECT
14	7	SYNCIN	I	Synchronization Pulse Input
15	-	N/C	-	NO CONNECT
16	8	V_{DD}	-	Positive Supply

PIN NAME CROSS-REFERENCE TO LXP60x Table 2

DS21600 DS21602 DS21604	LXP600A LXP602 LXP604	DESCRIPTION
SYNCOUT	FSO	Synchronization Pulse Output
CLKOUT2	HFO	Clock 2 Output
CLKIN	CLKI	Clock Input
CLKOUT1	CLKO	Clock 1 Output
V_{SS}	GND	Ground
SEL	SEL	Clock Mode Select
SYNCIN	FSI	Synchronization Pulse Input
N/C	N/C	NO CONNECT
V_{DD}	V_{CC}	Positive Supply

OPERATION

Mode Select

The SEL pin is used to select the operating frequencies. Table 3 shows the SEL state for the various operating modes of the DS21600, DS21602, and DS21604.

FREQUENCY CONVERSIONS (MHz) Table 3

	SEL	CLKIN	CLKOUT1	CLKOUT2
DS21600	**0**	1.544	2.048	6.144
	1	2.048	1.544	6.176
DS21602	**0**	1.544	2.048	8.192
	1	2.048	1.544	6.176
DS21604	**0**	1.544	4.096	8.192
	1	4.096	1.544	6.176

Frame Sync Input

In all cases, CLKOUT1 and CLKOUT2 are frequency-locked to CLKIN. CLKOUT1, CLKOUT2, and SYNCOUT are phased-locked to SYNCIN when SYNCIN is asserted. It will take a maximum of 100ms for this alignment to occur after the first instance of SYNCIN.

SYNCIN should be tied low when not used.

OUTPUT JITTER

The output jitter specifications are shown in Table 4 for 2.048MHz (or 4.096MHz) to 1.544MHz conversions (SEL = 1) and 1.544MHz to 2.048MHz (or 4.096MHz) conversions (SEL = 0).

OUTPUT JITTER SPECIFICATIONS Table 4

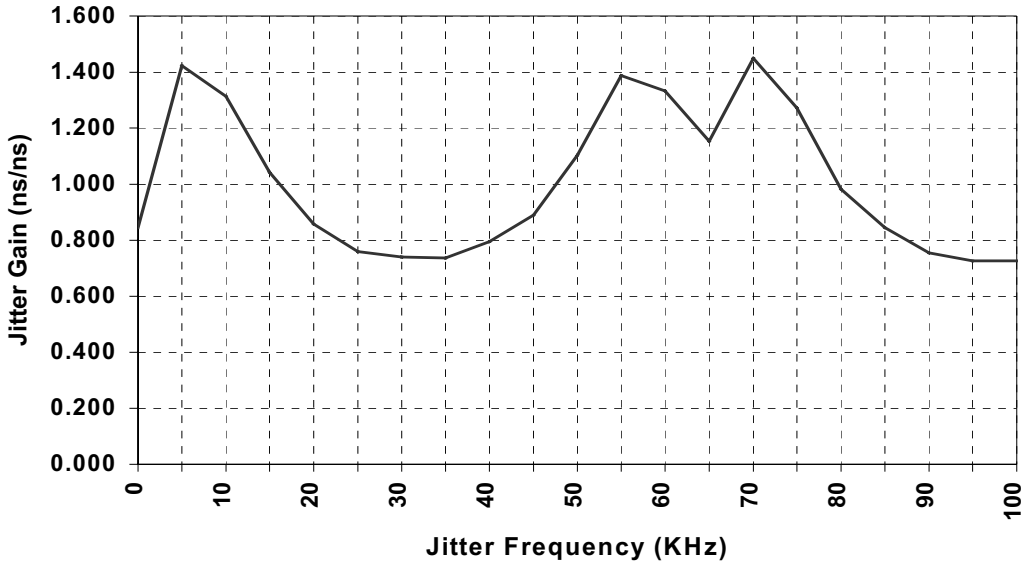
CLKIN	CLKOUT1	FREQUENCY BAND	SPECIFICATION	SPEC. VALUE	TYPICAL	MAX	UNITS
1.544MHz	2.048MHz	20Hz to 100kHz	G.823	1.500	0.012	0.035	UI pp
		18kHz to 100kHz	G.823	0.200	0.008	0.025	UI pp
2.048MHz or 4.096MHz	1.544MHz	No bandlimiting	TR62411	0.050	0.002	0.020	UI pp
		10Hz to 40kHz	TR62411	0.025	0.001	0.010	UI pp
		8kHz to 40kHz	TR62411	0.025	0.001	0.012	UI pp

Jitter Transfer

Jitter transfer for 2.048MHz to 1.544MHz conversion and vice versa are shown in Figure 2-1 and Figure 2-2.

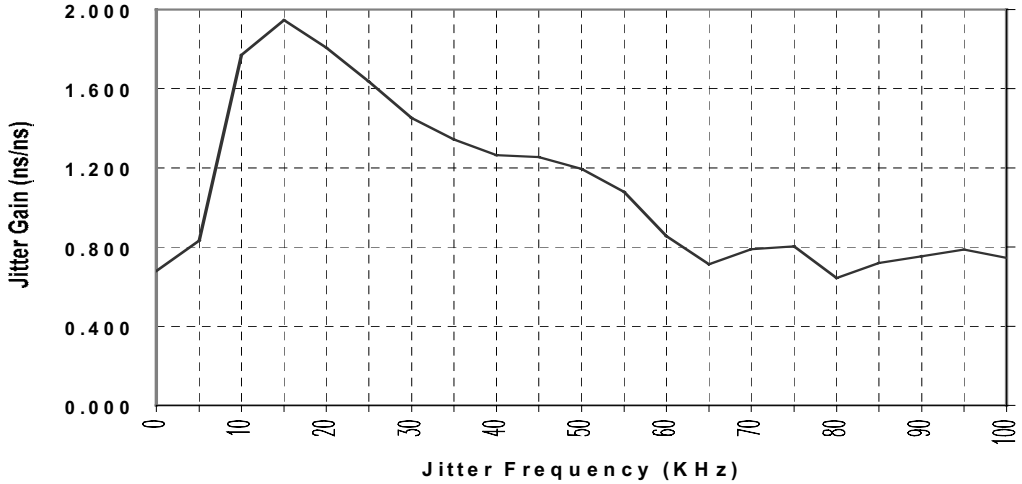
NOMINAL JITTER TRANSFER FOR 2.048MHz TO 1.544MHz CONVERSION

Figure 2-1



NOMINAL JITTER TRANSFER FOR 1.544MHz TO 2.048MHz CONVERSION

Figure 2-2



OPERATING PARAMETERS

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +6.0V
Operating Temperature for DS21600SN, DS21602SN, DS21604SN	-40°C to +85°C
Storage Temperature	-55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		5.5	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply for 5V Operation	V_{DD}	4.75	5	5.25	V	

DC CHARACTERISTICS (-40°C to +85°C; V_{DD} = 5.0V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current @ 5V	I_{DD}			8	mA	2
Input Leakage	I_{IL}	-1.0		+1.0	µA	1
Output Leakage	I_{LO}			1.0	µA	
Output Current (2.4V)	I_{OH}	-1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES:

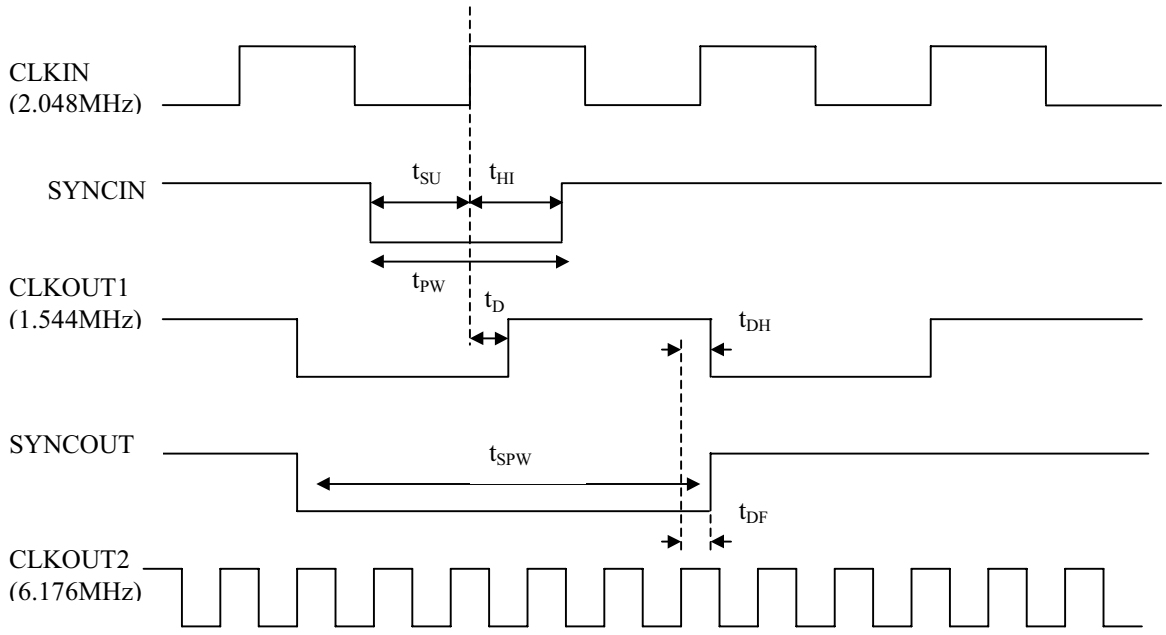
1. $0V < V_{IN} < V_{DD}$.
2. Outputs open.

AC TIMING

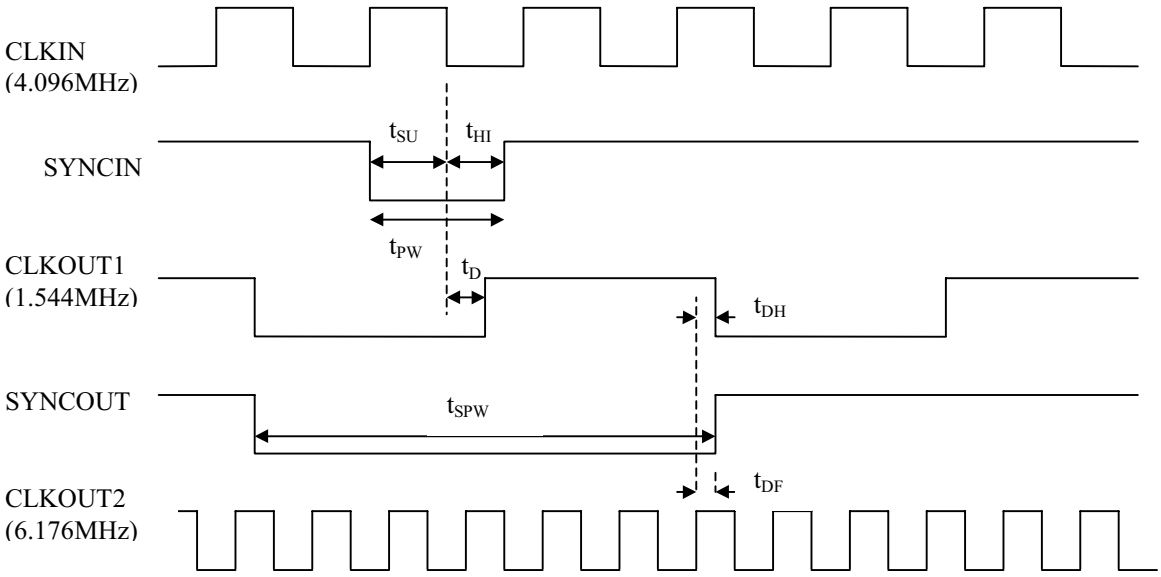
PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNIT	NOTES
Capture Range on CLKIN	-	±10,000	-	-	ppm	1
Lock Range on CLKIN	-	±10,000	-	-	ppm	1
CLKIN Duty Cycle	-	35	-	65	%	1
SYNCIN Setup to CLKIN Rising	t_{SU}	46	-	-	ns	
SYNCIN Hold After CLKIN Rising	t_{HI}	30	-	-	ns	
SYNCIN Pulse Width	t_{PW}	76	-	CLKIN period	ns	
CLKOUT1 Delay from CLKIN Rising	t_D	-15	0	+15	ns	
CLKOUT1 Duty Cycle	C_D	49	-	51	%	
SYNCOUT Pulse Width	t_{SPW}	-	-	CLKOUT1 period	ns	
SYNCOUT Delay from CLKOUT2	t_{DF}	-5	-	30	ns	
CLKOUT1 Delay from CLKOUT2	t_{DH}	-15	0	+15	ns	
Rise/Fall Time on CLKIN, SYNCIN	t_{RF}	-	-	40	ns	1
Rise/Fall Time on CLKOUT, SYNCOUT, CLKOUT2 with a 25pF Load	t_{RF}	-	-	40	ns	

1. Guaranteed by design

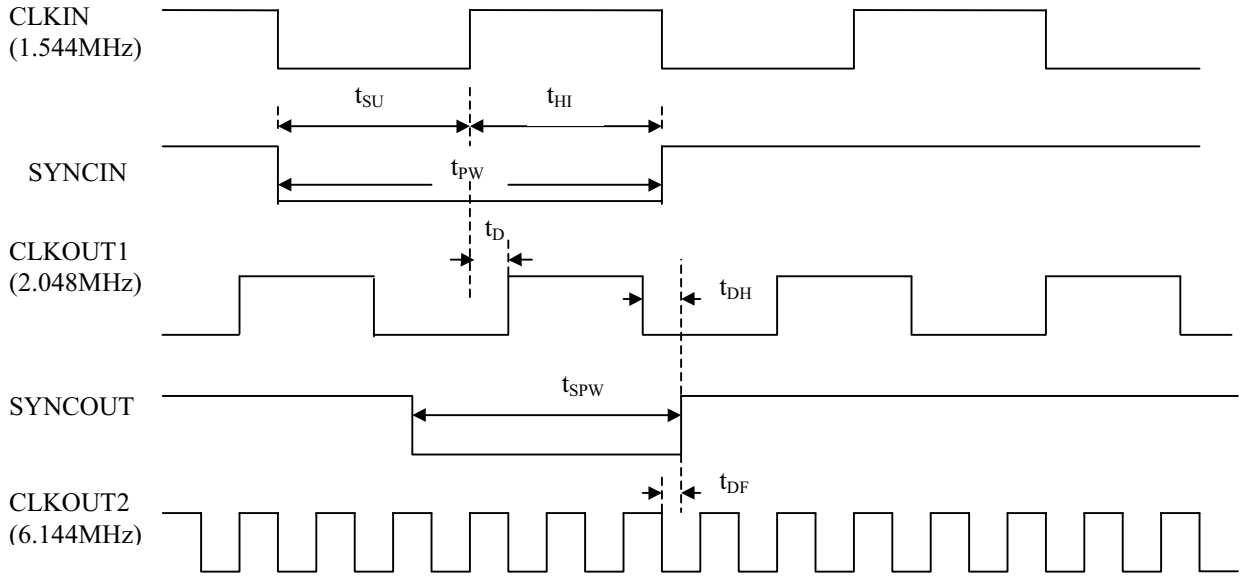
DS21600 AND DS21602 HIGH TO LOW FREQUENCY CONVERSION FRAME SYNC ALIGNMENT Figure 3-1



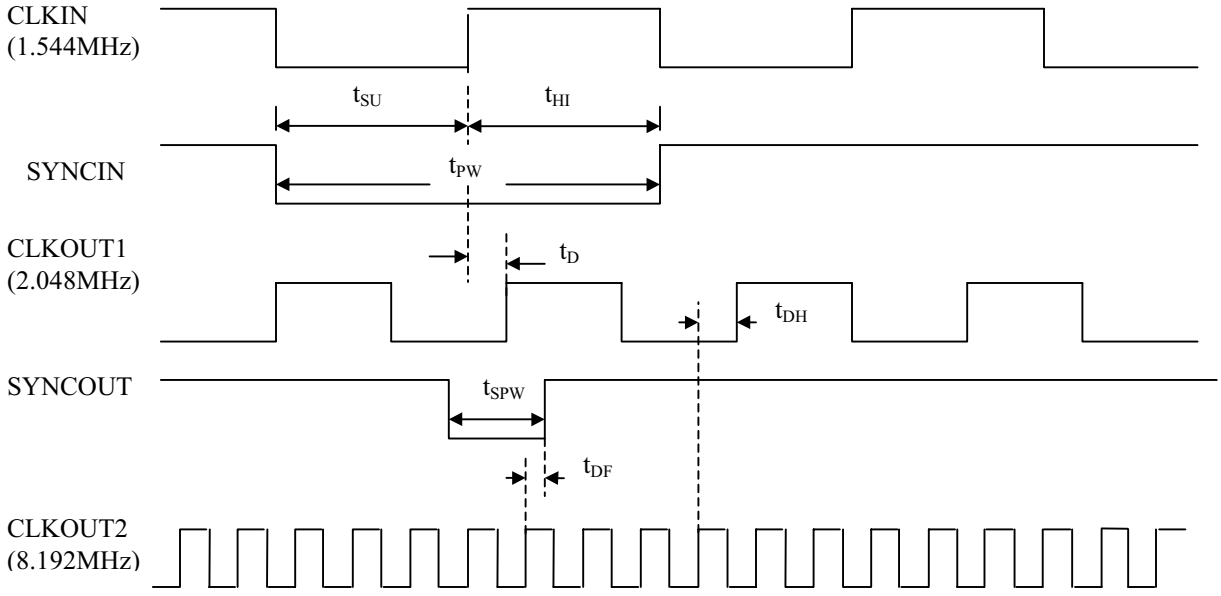
DS21604 HIGH TO LOW FREQUENCY CONVERSION FRAME SYNC ALIGNMENT Figure 3-2



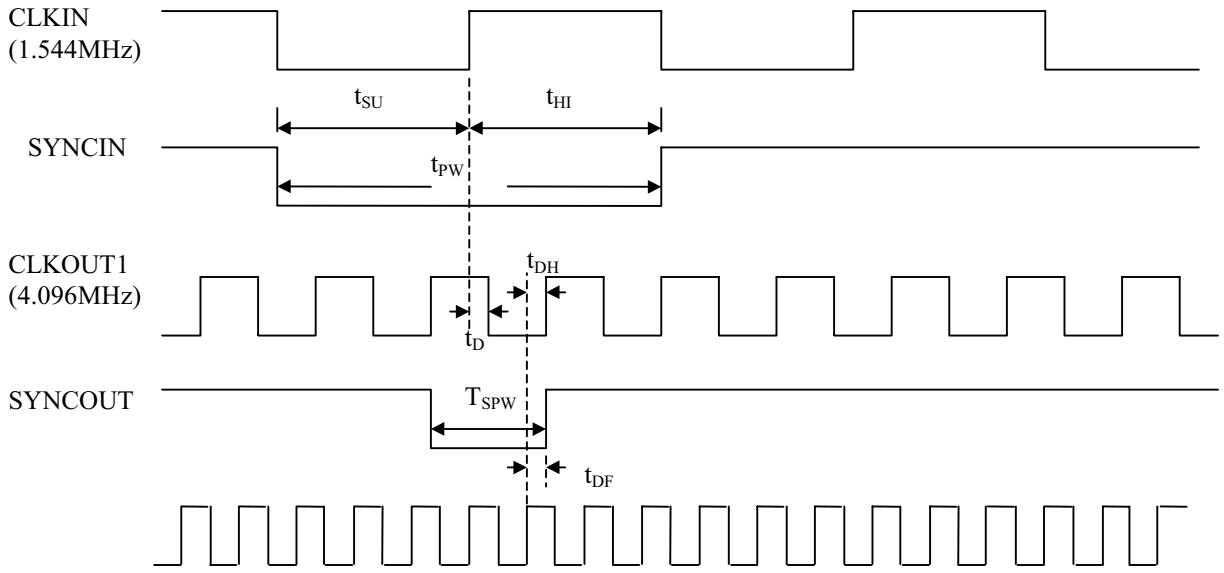
DS21600 LOW TO HIGH FREQUENCY CONVERSION FRAME SYNC ALIGNMENT Figure 3-3



DS21602 LOW TO HIGH FREQUENCY CONVERSION FRAME SYNC ALIGNMENT Figure 3-4

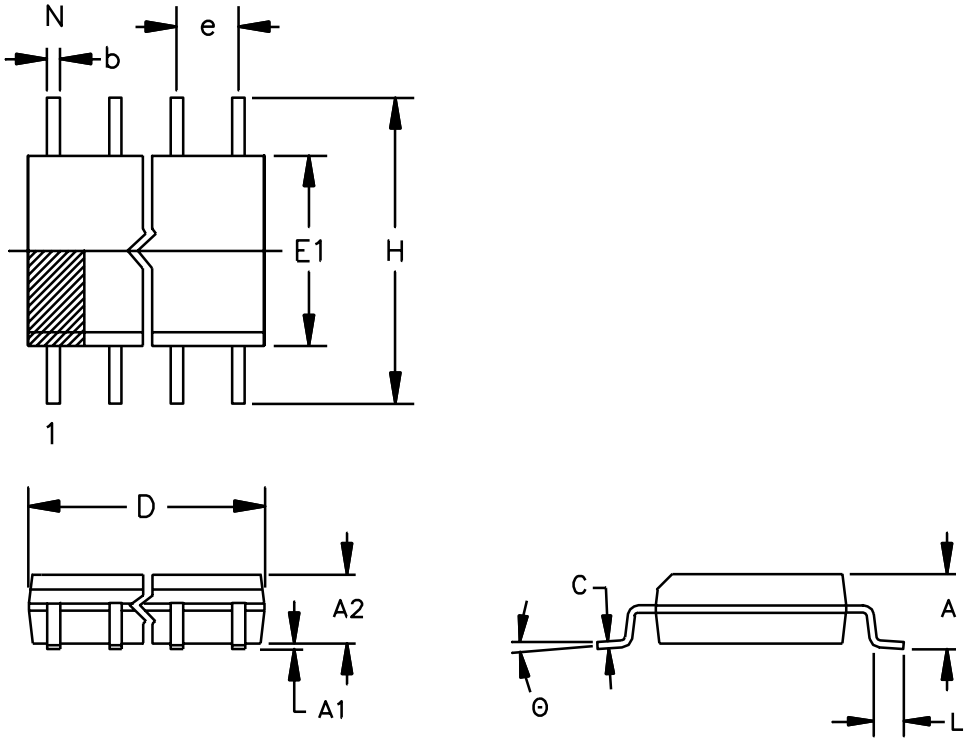


DS21604 LOW TO HIGH FREQUENCY CONVERSION FRAME SYNC ALIGNMENT Figure 3-5



PACKAGE SPECIFICATIONS

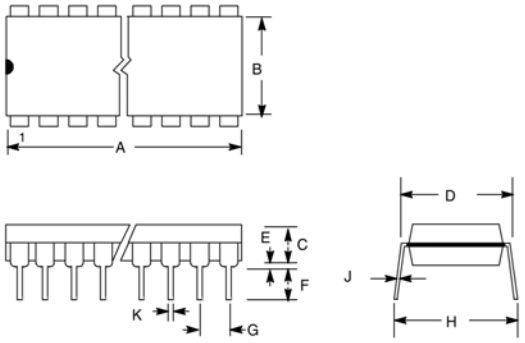
PACKAGE OUTLINE SOIC 16-PIN 0.300” BODY Figure 4



LTR		MIN	MAX
A	IN.	0.094	0.105
	MM	2.39	2.67
A1	IN.	0.004	0.012
	MM	0.102	0.30
A2	IN.	0.089	0.095
	MM	2.26	2.41
b	IN.	0.013	0.020
	MM	0.33	0.51
C	IN.	0.009	0.013
	MM	0.229	0.33
D	IN.	0.398	0.412
	MM	10.11	10.46
e	IN.	.050 BSC	
	MM	1.27 BSC	
E1	IN.	0.290	0.300
	MM	7.37	7.62
H	IN.	0.398	0.416
	MM	10.11	10.57
L	IN.	0.016	0.040
	MM	0.40	1.02
Θ		0°	8°

THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A TERMINAL 1 IDENTIFIER MUST BE POSITIONED IN THE HATCHED ZONE.

PACKAGE OUTLINE 8-PIN DIP (300-MIL) Figure 5



PKG	8-PIN	
DIM	MIN	MAX
A IN. MM	0.360 9.14	0.400 10.16
B IN. MM	0.240 6.10	0.260 6.60
C IN. MM	0.120 3.05	0.140 3.56
D IN. MM	0.300 7.62	0.325 8.26
E IN. MM	0.015 0.38	0.040 1.02
F IN. MM	0.120 3.04	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN MM	0.320 8.13	0.370 9.40
J IN MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

REVISION HISTORY

1. Preliminary release, 082100.
2. Added package specifications, 083100.
3. Correct operating voltage range, 090100.
4. Added mechanical drawing for DIP package, 011101.
5. Added jitter specifications and pin list for all packages; added timing diagrams, 092801.